

WHAT IS CLAIMED IS:

1. A cache memory system including a small-capacity cache memory which enables high-speed access and is provided between a processor and a main memory, comprising:

a software cache controller which performs software control for controlling data transfer to the cache memory in accordance with a preliminarily programmed software; and

a hardware cache controller which performs hardware control for controlling data transfer to the cache memory by using a predetermined hardware;

wherein the processor causes the software cache controller to perform the software control but causes the hardware cache controller to perform the hardware control when it becomes impossible to perform the software control.

2. A cache memory system according to Claim 1, wherein when a cache miss happens at the time of the software control, the processor causes the hardware cache controller to perform the hardware control.

3. A cache memory system according to Claim 1, wherein the software cache controller stores desired data in the cache memory in accordance with a code produced by static prediction of a compiler.

4. A cache memory system according to Claim 2, wherein the software cache controller stores desired data in the cache memory in accordance with a code produced by static prediction of a compiler.

5. A cache memory system according to Claim 3, wherein before the processor executes a data read-out instruction for reading out desired data of the main memory, the software cache controller reads out data at an address of the main memory designated by the data read-out instruction and stores the data in

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the cache memory.

6. A cache memory system according to Claim 4, wherein before the processor executes a data read-out instruction for reading out desired data of the main memory, the software cache controller reads out data at an address of the main memory designated by the data read-out instruction and stores the data in the cache memory.

7. A cache memory system according to Claim 5, wherein at the same time when the processor executes the data read-out instruction, the software cache controller transfers from the cache memory to the processor the data at the address of the main memory designated by the data read-out instruction.

8. A cache memory system according to Claim 6, wherein at the same time when the processor executes the data read-out instruction, the software cache controller transfers from the cache memory to the processor the data at the address of the main memory designated by the data read-out instruction.

9. A cache memory system according to Claim 3, wherein before the processor executes a data write instruction for writing data in the main memory, the software cache controller designates an address of the cache memory, which is used for storing data from the processor.

10. A cache memory system according to Claim 4, wherein before the processor executes a data write instruction for writing data in the main memory, the software cache controller designates an address of the cache memory, which is used for storing data from the processor.

11. A cache memory system according to Claim 9, wherein when the processor executes the data write instruction, the data from the processor written at the designated address the cache memory is written by the software cache

controller at an address of the main memory designated by the data write instruction.

12. A cache memory system according to Claim 10, wherein when the processor executes the data write instruction, the data from the processor written at the designated address the cache memory is written by the software cache controller at an address of the main memory designated by the data write instruction.

13. A cache memory system according to Claim 1, wherein the hardware cache controller performs line management of the cache memory by using a set-associative method for multiple ways and the software cache controller performs line management of the cache memory by using a fully associative method for at least one way in the multiple ways.

14. A cache memory system according to Claim 2, wherein the hardware cache controller performs line management of the cache memory by using a set-associative method for multiple ways and the software cache controller performs line management of the cache memory by using a fully associative method for at least one way in the multiple ways.

15. A cache memory system according to Claim 3, wherein the hardware cache controller performs line management of the cache memory by using a set-associative method for multiple ways and the software cache controller performs line management of the cache memory by using a fully associative method for at least one way in the multiple ways.

16. A cache memory system according to Claim 4, wherein the hardware cache controller performs line management of the cache memory by using a set-associative method for multiple ways and the software cache controller

performs line management of the cache memory by using a fully associative method for at least one way in the multiple ways.

17. A cache memory system according to Claim 1, wherein the software cache controller is formed by a transfer control processor for controlling data transfer to the cache memory.

18. A cache memory system according to Claim 2, wherein the software cache controller is formed by a transfer control processor for controlling data transfer to the cache memory.

19. A cache memory system according to Claim 3, wherein the software cache controller is formed by a transfer control processor for controlling data transfer to the cache memory.

20. A cache memory system according to Claim 4, wherein the software cache controller is formed by a transfer control processor for controlling data transfer to the cache memory.

21. A cache memory system according to Claim 13, wherein the software cache controller is formed by a transfer control processor for controlling data transfer to the cache memory.

22. A cache memory system according to Claim 14, wherein the software cache controller is formed by a transfer control processor for controlling data transfer to the cache memory.

23. A cache memory system according to Claim 15, wherein the software cache controller is formed by a transfer control processor for controlling data transfer to the cache memory.

24. A cache memory system according to Claim 16, wherein the software cache controller is formed by a transfer control processor for controlling

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data transfer to the cache memory.

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